Appl. No. 10/649,076
Amdt. dated March 23, 2005
Reply to Office action of December 23, 2004

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A memory, comprising:
   a first magnetic memory element;
   a first group of conductors magnetically coupled to the first magnetic memory element;
   a second magnetic memory element; and
   a second group of conductors magnetically coupled to the second magnetic memory element;
   wherein ~~the second memory element is substantially vertical to the first memory element, and~~ the first and second group of conductors have at least one conductor in common; and
   wherein a magnetic field is induced in the first and second memory elements using the common conductor, and wherein the induced field temporarily perturbs a resistance of the first and second memory elements.

2. (Original) The memory of claim 1, wherein the magnetic memory elements are capable of having their magnetic orientation adjusted by the common conductor.

3. (Original) The memory of claim 2, wherein power required to change magnetic orientation of the magnetic memory elements is dependant on the number of conductors, and wherein the number of conductors used for writing data to the memory elements is three or less.

4. (Original) The memory of claim 2, wherein the memory elements are written to a digital state by inducing current in the common conductor, and then

the memory elements are selectively written to opposite digital states by inducing a current in the common conductor and inducing a current in a conductor that is not common to the memory elements.

5. (Original) The memory of claim 2, wherein the orientation of the magnetic memory elements are adjusted independently.

6. (Original) The memory of claim 1, wherein the magnetic memory elements further comprise hard axis magnetization thresholds that are altered.

7. (Original) The memory of claim 1, wherein the magnetic orientation of the memory elements are sensed while current flows in the common conductor.

8. (Original) The memory of claim 7, wherein read and write operations are performed simultaneously.

9. (Original) The memory of claim 1, wherein the common conductor is between the memory elements.

10. (Currently amended) A method, comprising:
monitoring a plurality of memory elements to measure a rate of change of resistance of the memory elements, ~~wherein the memory elements are substantially vertical~~;
providing a magnetic field to the memory elements using a conductor that is magnetically coupled to at least two memory elements; and
determining a digital state by monitoring the memory elements while the magnetic field is ~~switched~~ perturbed.

11. Canceled.

12. Canceled.

13. (Original) The method of claim 10, wherein the original magnetic orientation of the memory elements is not changed by the provided magnetic field.

14. (Currently amended) A computer, comprising:
a processor;
a bridge logic device coupled to said processor;
a memory coupled to the processor, comprising:
a plurality of magnetic memory elements ~~that exist on separate planes~~; and
a conductor magnetically coupled to the plurality of memory elements ~~that are on separate planes~~
wherein a current digital state of at least one of the plurality of memory elements is determined by monitoring resistance of the at least one memory element while magnetic orientation of the at least one memory element orientation is perturbed.

15. Canceled.

TP 16. (Original) The memory of claim ~~15~~ 14, wherein the conductor provides independent control of the digital state of the memory elements.

17. (Currently amended) A method, comprising:
providing a common conductor to a plurality of memory elements, wherein the common conductor magnetically couples to the memory elements;
inducing a magnetic field by flowing a current in the common conductor; ~~and~~
~~altering~~ perturbing ~~the~~ a digital state of the memory elements using the induced magnetic field; and

monitoring a resistance of the memory elements while altering a digital state of the memory elements.

~~wherein the memory elements are not part of the same plane.~~

18. Canceled.

19. Canceled.

20. (Currently amended) A computer, comprising:
a processor;
a bridge logic device coupled to said processor;
a means for storing and retrieving information that is coupled to the processor, wherein the means for storing and retrieving information comprises:
a first magnetic memory element;
a second magnetic memory element arranged adjacent to ~~vertically stacked above~~ the first magnetic memory elements; and
a conductor coupled to both the first and second magnetic memory elements, wherein the conductor is adapted to switch a magnetic orientation of ~~the first magnetic memory element, the second magnetic memory element and~~ both the first and second magnetic memory elements while determining a current digital state of the first and second memory elements.

21. (New) The method of claim 17, wherein a rate of change of the resistance indicates the digital state of the memory elements.

22. (New) The method of claim 21, wherein perturbing the digital state does not change a magnetic orientation of the memory element.

23. (New) The memory of claim 1, wherein a digital state of each memory element is determined by monitoring a rate of change of the perturbed resistance.

24. (New) The memory of claim 23, wherein the digital state is a current digital state stored in the memory element.

25. (New) The method of claim 10, wherein the digital state is a current digital state stored in the memory element.

26. (New) The method of claim 10, wherein a rate of change of the resistance indicates the digital state of the memory elements.